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TITLE **A PROGRAMMABLE MULTICHANNEL CORRELATION MODULE FOR ANALYZING NEUTRON MULTIPLICITIES**

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A PROGRAMMABLE MULTICHANNEL CORRELATION MODULE FOR ANALYZING NEUTRON MULTIPLICITIES

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Abstract

We have developed a CAMAC module for analyzing neutron multiplicities. Reduction in dead time over previous methods has been made possible by providing independent detector channels. We have achieved a considerable reduction in circuitry by utilizing RAM and PROM integrated circuits in a nonstandard fashion. Along with specially developed algorithms, the module has been able to successfully unfold overlapping multiplicity chains for count rates varying over three orders of magnitude.

I. INTRODUCTION

The programmable multichannel correlation module (PMCCM) is a double-wide CAMAC module designed to process pulses from several neutron detectors. This module allows detection and quantification of coherent neutrons that identify the presence of spontaneously fissioning isotopes.

The basic technique for quantifying coherent neutron pulses involves simulating a time window with a clocked shift register and counting the number of pulses entering the shift register. Then, as each pulse exits the shift register, the remaining pulses are recorded in histogram form.

A major design objective of the PMCCM, as it applies to earlier designs of this type [1-2], was to lower the overall dead time. We accomplished this by providing, in effect, a separate shift register for each detector channel and by minimizing the time that each channel input is disabled from processing input pulses. This dead time is 12 ns per shift register clock. Earlier designs summed the output of several detectors, then sent it to one shift register, which meant that once a pulse was loaded into the shift register, the unit could no longer accept pulses until the existing pulse was shifted into the next bin. Another design objective was to make a module that could be easily adapted to different detector types and configurations. We met this objective by making the module's key parameters software programmable.

II. MODULE DESCRIPTION

The PMCCM comprises the following components and their operations (see Fig. 1).

- The oscillator generates the overall PMCCM system timing and drives the programmable clock circuit and the programmable background read clock circuit.

- The programmable clock, which generates the shift register clock signal, can be programmed to be 2 MHz, 1 MHz, 500 kHz or 250 kHz, thus providing a clock period or shift register bin time of 500 ns, 1 μs, 2 μs, or 4 μs, respectively.

- The input synchronizer latches pulses (hits) that occur on any of the 15 inputs of the PMCCM module. Only one pulse per channel can be latched every clock period. The inputs to the PMCCM can be disabled via the CAMAC interface.

- The summing PROM basically sums the number of input channels hit during the current clock period and produces a 4-bit binary value (data byte) from 0-15. The output of this circuit is sent to the shift register and the up/down counter via the adder.

- The programmable shift register (Fig. 2) shifts the data byte received for each clock period. The shift register length is programmable from the range of 1-1024 bins. The shift register bin time is based upon the setting for the programmable clock, which ranges from 500 ns to 4 μs. The shift register consists of a standard 1024 by 4 static RAM chip, whose address lines are driven by a 10-bit binary counter. The shift register length is programmed by loading the desired value into the length register. The output of the binary counter and the output of the length register are compared by a 10-bit comparator, when the two are equal, the binary counter is reset to zero. In effect, a data byte is loaded into RAM sequentially at the rate determined by the shift register clock (SR

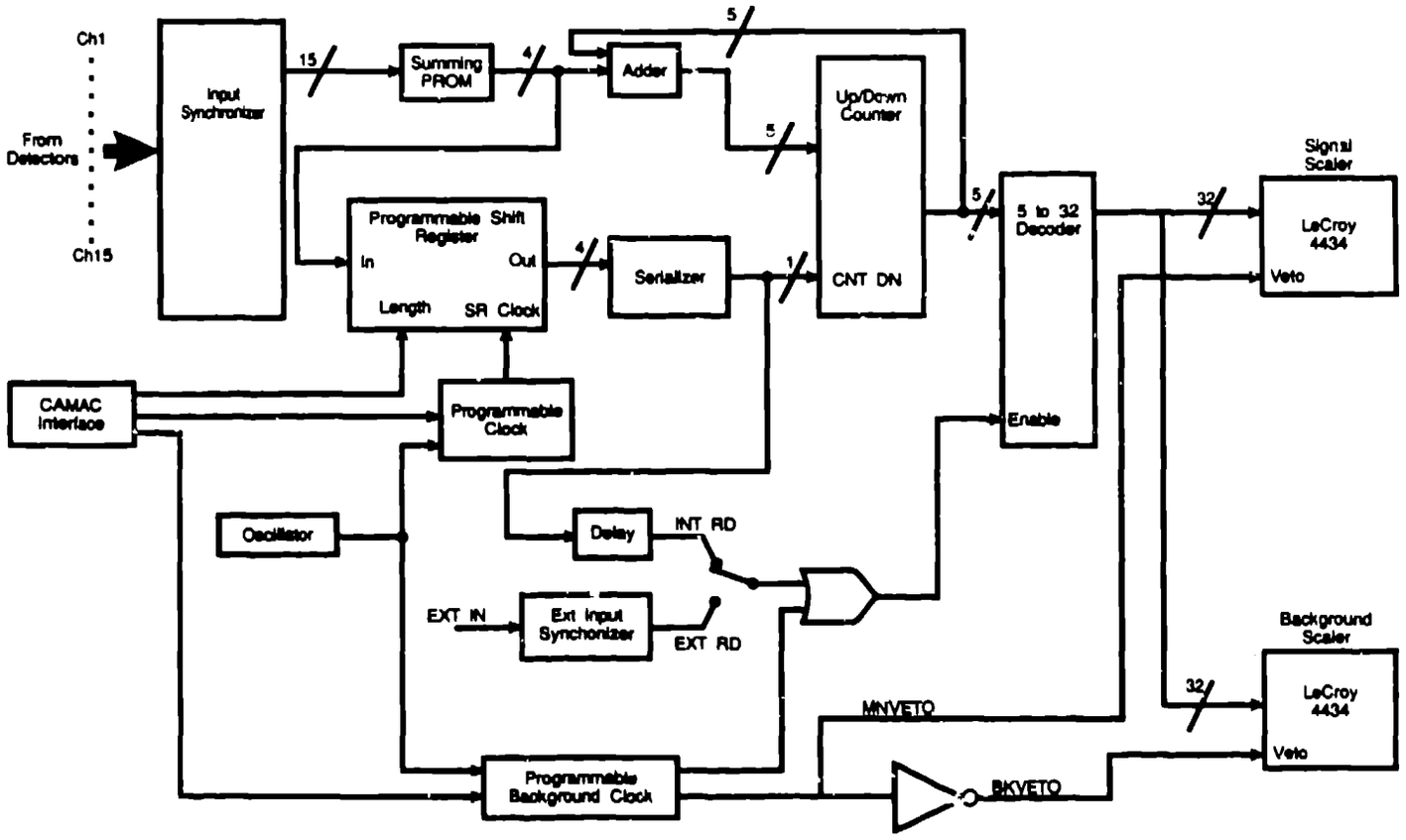


Fig. 1. Block diagram of the PMCCM.

Clock). Thus, during one SR Clock period, the current memory location is read out and loaded into the serializer, then the data byte from the summing PROM is loaded into the same memory location.

• The up/down counter stores the sum of data bytes that are contained in the shift register. As the data bytes are shifted into the shift register, they are also added to the up/down counter via the adder. As the data byte is shifted out, it is converted into a pulse stream by the serializer. This serial stream of pulses down counts or subtracts from the up/down counter one pulse at a time, whereas the add portion of the cycle adds a number from 0-15 to the up/down counter in one operation. The maximum count value maintained in the up/down counter can be as high as 255, although only a value of 0-31 is decoded. An overflow/underflow error will occur if the up/down counter ever underflows 0 or exceeds 31. This error will illuminate the "E" LED on the front panel and an provide error status in the CAMAC status word.

• The 5- to 32-channel decoder is used to decode the up/down counter value and route a pulse out of the appropriate scaler channel signal line to the selected Lecroy 32-channel scaler module.

• Both the signal and background scalers are Lecroy Model 4434 CAMAC scaler modules. Each of these units contains 32 separate 20-MHz scalers that are 24-bits deep. The PMCCM's 32-channel outputs are bused to the 32-channel inputs of each Lecroy 4434. Only one of the scaler units is enabled at a time. This is accomplished by using the MNVETO and BKVETO signal provided by the PMCCM to enable each of the scalers via their VETO inputs.

• The INT RD\EXT RD switch, located on the front panel, determines how the up/down counter value will be sent to the signal scaler. The status of this switch can also be obtained via the CAMAC interface. If this switch is in the INT RD mode, the up/down counter

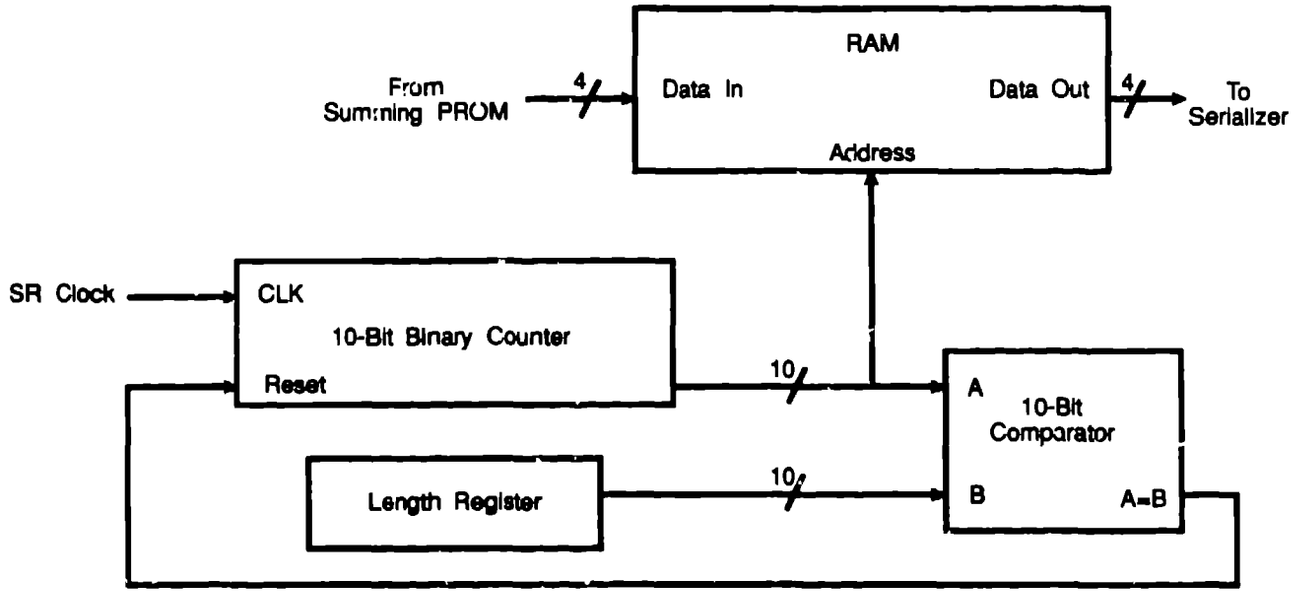


Fig. 2. Block diagram of the programmable shift register.

value will be read out each time a down count is sent out of the serializer. The up/down counter will be decremented first, then a pulse will be sent to the appropriate up/down scaler channel. If the switch is in the EXT RD position, a pulse injected into the EXT RD input will make the reading. (This is discussed in more detail in Sec. III.)

• The background clock circuitry controls the background read synchronization. The up/down counter to the background scaler is read out at a programmed rate. The interval at which this read occurs is programmed to one of the following intervals: 8 μs, 32 μs, 128 μs, 512 μs, 2.048 ms, 8.192 ms, 32.768 ms, 131.072 ms, 524.288 ms, 2.097 s, 8.388 s, 33.554 s, 134.217 s, 536.87 s, and 2147.48 s. The background read can also be disabled via a CAMAC command.

• The CAMAC interface circuitry is used to interface the PMCCM with the CAMAC bus, which allows the CAMAC controller (under software control) to program the PMCCM and read its status. The CAMAC interface performs the following functions.

1. Programs the shift register length.
2. Programs the shift register clock frequency.
3. Programs the background clock frequency.
4. Enables and disables CH0-CH15 inputs.
5. Resets counters, shift register, error latch, etc.
6. Reads the status of the error latch.
7. Reads the status of the INT RD\EXT RD switch.
8. Reads the status of the diagnostic switch.

III. MODES OF OPERATION

The front panel INT/EXT RD switch selects the PMCCM operational modes. If EXT is selected then external read pulses are fed into the EXT RD INPUT. All the experiments described in this document used the internal read mode.

A. Internal Read Mode

If a pulse or packet of pulses is shifted out of the shift register via the serializer, the up/down counter will be decremented by one for each pulse and then a pulse will be sent out to the signal scaler module. The channel (CH) in which the pulse occurs corresponds to the value in the up/down counter after it was decremented. For example, if the up/down counter had a value of 1 at the beginning of the down count cycle and a single down count is obtained from the shift register via the serializer, the up/down counter is first decremented to 0 and then a pulse is sent from the CH0 signal line to the signal scaler.

The largest acceptable packet of down counts that can occur at a given clock cycle is 15. For the following example, let us assume a count of 15 is in the up/down counter and the down count packet is equal to 15. First, the up/down counter is decremented by 1, making it equal to 14; next, a pulse is sent out the CH14 signal line, and the up/down counter is decremented by 1, making it 13; then a pulse is sent out the CH13 signal line. This progression continues until the up/down counter is decremented by the 15th down pulse at which time the up/down counter will be decremented to 0. A pulse is then sent out the CH0 signal line. It should also be noted that if no down count pulses are shifted out of the shift register via the serializer, there will be no pulses sent to the up/down counter. The pulses are sent out of the serializer at 40 MHz.

After the down count portion of the cycle is completed, the number of input channel hits are added to the up/down counter; this number can be 0-15. This data byte is also put into the shift register and will eventually reach the output of the shift register, where it will be used to down count the up/down counter and send pulses to the signal scaler unit. The time at which the data byte arrives at the output is based on the product of the shift register clock period and the number of shift register bins used, both of which are programmable. This time ranges from 500 ns for a clock period of 500 ns and shift register length of 1 to a maximum time of 4.096 ms for a clock period of 4 μs and shift register length of 1024.

The value of the up/down counter is also read out during background reads. Instead of reading out the up/down counter value to the signal scaler, the value is sent to the background scaler. This occurs once during every background read time (i.e., the programmable submultiple of the oscillator frequency). For example, if during a background read the up/down counter contains the number 12, then a pulse will be sent out the CH12 signal line to the background scaler unit. The signal scaler unit will be disabled via the MNVETO signal and the back scaler unit will be enabled via the BKVETO signal.

B. External Read Mode

The external read mode is very similar to the internal read mode with one major exception: instead of the down pulses to the up/down counter generating the pulses sent to the signal scaler, an external read pulse will generate the pulse sent to the signal scaler. When a pulse is detected on the external read input during the cycle, it is latched and used to enable an up/down counter read once that cycle. The read takes place after the down count and add portions of the cycle. Basically, if an external read pulse occurs, the value of the up/down counter will be sent out the appropriate line to the signal scaler.

C. PMCCM's Performance

Pulsing all 15 inputs with the same signal is an acid test of the PMCCM's ability to process overlapping pulses. The pulses are correctly counted as a 15-fold event 99.4% of the time. The 0.6% loss is due to a 12-ns dead time at the boundary between adjacent 2-μs time bins.

IV. TYPICAL DATA REDUCTION

To unfold overlapping neutron clusters and remove the effects of random neutrons, several numerical steps must be taken (see Ref. 3 for more details).

We configured the shift register for a time span equaling about 4 "half-lives" of the detector system. Four half-lives span about 94% of the coincident probability envelope, which reduces the detector efficiency for detecting coincidences 6%.

It is important to distinguish between the two sets of data. In the first data set (in the signal scalers), the up/down scaler is read because a neutron pulse triggered the read function, and the following pulses in the shift register may be correlated with the trigger neutron by having been born in the same (or a concatenated) fission. In the second data set (in the background scalers), the pulses in the shift register cannot be correlated with the trigger, because the trigger was merely an arbitrary electronic signal having nothing to do with the fission process.

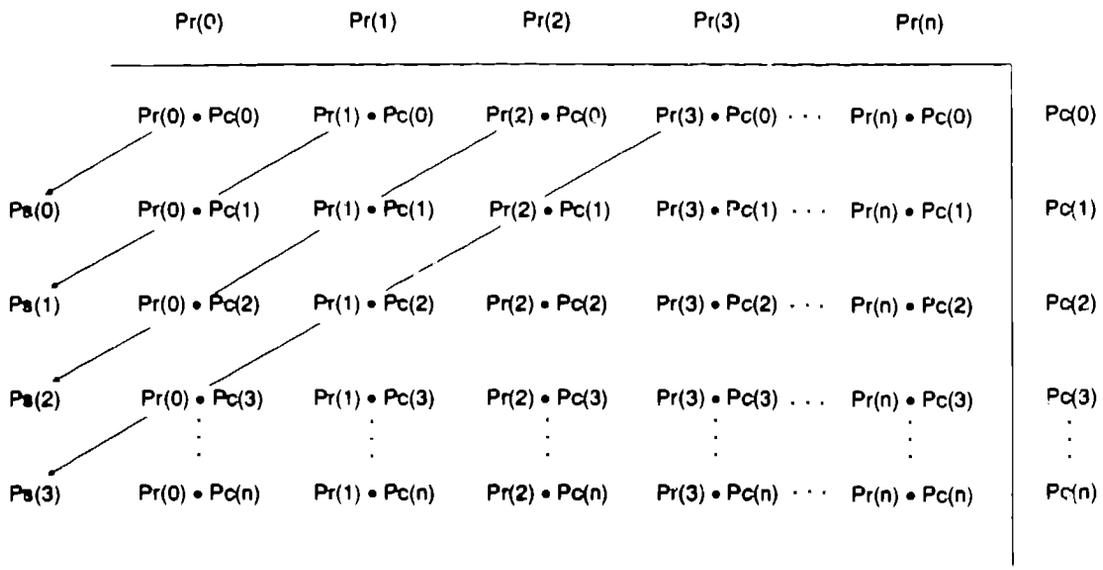
The desired coincident probabilities are obtained by the following numerical steps.

1. The histogram of discrete events stored in the 32 signal scalers is reduced by normalization to a set of probabilities, $P_s(n)$, that exactly 0, 1, 2,...n pulses are found in the shift register when the read function is triggered by a neutron pulse exiting the shift register.

2. The histogram of discrete events stored in the 32 background scalers is reduced by normalization to a set of probabilities, $P_r(n)$, that exactly 0, 1, 2,...n pulses are found in the shift register when the read function is triggered by an arbitrary electronic pulse.

3. These two sets of probabilities are then combined to extract the probabilities, $P_c(n)$, that a neutron pulse trigger finds 0, 1, 2,...n correlated pulses in the shift register.

Consider the following matrix:



The $P_r(i)$ across the top are the probabilities obtained from the background histogram; the $P_c(j)$ down the right side are the unknown correlated probabilities that we seek. Each matrix entry is the product of the column head multiplied by the right margin term: $P_r(i) \times P_c(j)$. In the left margin, we have the $P_s(n)$ values, which are the probabilities of finding n neutron pulses in the shift register given a neutron trigger.

Clearly, $P_s(0) = P_r(0) \times P_c(0)$, because n = 0 only if no random pulses and no correlated pulses are observed. Hence, $P_c(0) = P_s(0)/P_r(0)$, and we have the zero term in the $P_c(n)$ array. For the case in which only one coincident neutron is detected, we have

$$P_s(1) = P_r(1) \times P_c(0) + P_r(0) \times P_c(1) \qquad (1)$$

Equation 1 arises from the fact that a single coincident pulse can be observed in exactly two mutually exclusive ways:

a. One pulse uncorrelated with the trigger, and no pulse correlated with the trigger, or

b. No uncorrelated pulse and one correlated pulse.

If we rearrange Eq. 1, we have

$$P_c(1) = \frac{P_s(1) - P_r(1) \times P_c(0)}{P_r(0)} \qquad (2)$$

where we have used the $P_c(0)$ previously obtained. Summing along each diagonal (upper right to lower left) gives the total probability for observing exactly n pulses in the shift register. Each of these equations may be solved in turn for another term in $P_c(n)$.

The general expression for the correlated probabilities is

$$P_c(i) = \frac{P_s(i) - \sum_{j=0}^{i-1} P_c(j) \times P_r(i-j)}{P_r(0)} \qquad (3)$$

We need to emphasize that Pc(n) is the probability that a neutron pulse as it exits the shift register will "see" n correlated pulses in the shift register. By "correlated" we mean pulses arising from the detection of neutrons born in the same fission as the trigger neutron or in a concatenated fission. It is important to note that Eq. 3 requires repeated subtraction with the result that there are large uncertainties associated with the probabilities for higher multiplicities.

4. There is one final step in reducing the data. Let us assume that the detector sees an isolated group of four correlated neutrons. These four pulses proceed through the shift register. The first to exit causes a read operation that sees the three following pulses, which increases the reading of the no. 3 signal scaler by 1. The next pulse exiting will have only two followers, and scaler no. 2 will increase by 1.

Similarly, the remaining two pulses will cause scalers no. 1 and 0 to increase.

We see that any group of n correlated pulses will be tallied in the (n-1)th scaler (one pulse is the trigger) and in every lower scaler. The last correction is to remove this overlap:

$$P_f(n) = P_c(n) - P_c(n+1) \quad . \tag{4}$$

and normalize the Pf(n) to unity. Thus, we have $P_f(n)$ as the probability of detecting clusters of n+1 correlated neutrons.

We now define some parameters used to characterize clusters. These parameters are count rate independent unless dotted (e.g., $\dot{M}1$ is M1 times the cluster trigger rate). One characteristic of an average cluster is the first moment obtained as follows:

$$M1 = \sum_{j=1} P_f(j) \, x \, j \quad . \tag{5}$$

Thus, M1 is the average number of extra pulses; that is, correlated pulses per cluster when considering the first pulse of a cluster as an independent event. Each spontaneous fission carries the same probability of "extra" neutrons; therefore,

$$\dot{M}1 = M1 \; x \; cluster \; trigger \; rate \tag{6}$$

should be proportional to the spontaneous fission source strength if the numerical process outlined above successfully corrects for the overlapping of pulse clusters.

We also generate a second (reduced) moment:

$$M2 = \sum_{j=2} P_f(j) \, x \, j(j-1) \quad , \tag{7}$$

which is also a cluster characteristic, but with quadratic weighting. Similarly, the product

$$\dot{M}2 = M2 \; x \; cluster \; trigger \; rate \tag{8}$$

is proportional to source strength. The $\dot{M}1$ and $\dot{M}2$ should be constant if a random source [e.g. (α,n)] is added to the spontaneous source, because a truly random source cannot contribute coherent events, even though it may contribute many triggers.

We also calculate M3 and M4, the third and fourth reduced moments, respectively. In many cases these moments are not supported by enough statistics to make them meaningful. However, they can be very significant where there is some multiplication (i.e., 1.1).

Linearity with Respect to Source Strength

Measurements to explore this point were made with a series of ^{252}Cf sources. Figure 3 displays the cluster parameters M1 and M2 as functions of count rate. For convenience, the points are plotted on an arbitrary logarithmic vertical scale, and no relationship between sets of points should be inferred. Their stability over a range of three decades indicates that the equipment and numerical procedure are reasonably successful in compensating for cluster overlap.

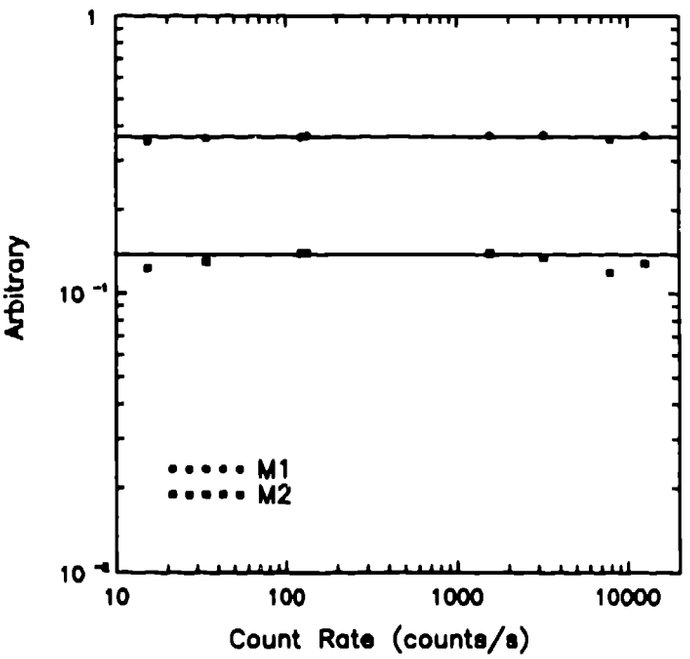


Fig. 3. Cluster parameters M1 and M2 are stable over widely varying count rates.

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